Attorney's Docket No.: 042390.P17013

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Louis A. Lippincott, et al.

Serial No.: 10/611,377

Filed: June 30, 2003

For: **CONTROLLING MEMORY ACCESS DEVICES IN A DATA DRIVEN ARCHITECTURE MESH ARRAY**

Examiner: Johnson, Brian P.

Art Group: 2183

Confirmation No.: 1508

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Appellants submit the following Appeal Brief pursuant to 37 C.F.R. § 41.37(c) for consideration by the Board of Patent Appeals and Interferences. The Appellants authorize the amount of $540.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f) to be charged to Deposit Account No. 02-2666.

I. REAL PARTY IN INTEREST

The Intel Corporation of Santa Clara, California obtained all rights to the subject application *via* the assignments recorded January 9, 2004 (Reel/Frame 014865/0774). Thus, as the owner at the time the brief is being filed, The Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, be directly affected by or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

Claims 1-9 and 11-29 are pending and rejected in the Application. Claim 10 has been cancelled. The Appellants respectfully appeal the rejections of claims 1-9 and 11-29.

IV. STATUS OF AMENDMENTS

No amendments were submitted after the Final Office Action mailed on October 14, 2008.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The references below to paragraph numbers and figures are to the Appellants' Specification as filed.

Claim 1 relates to a data driven processing method. The method comprises: providing a first set of instructions and incoming data to a first processing unit, of a data driven processor, to operate upon said incoming data (see paragraph [0039]; Fig. 8, item 804); configuring a data path for transferring data between a second processing unit of the data driven processor and external memory (see paragraphs [0039] and [0040]; Fig. 8, items 804 and 808); and the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing

to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second processing unit via said data path (see paragraphs [0039] and [0040]; Fig. 8, items 804 and 808).

Claim 5 relates to a data processor. The data processor comprises: a first direct memory access (DMA) unit (see paragraphs [0039] and [0040]; Fig. 8, items 804 and 808); and a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the DMA unit, the plurality of processing units are essentially identical units each having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port wherein the input port is programmable to route incoming data to any one of the output ports (see paragraphs [0017], [0019], and [0026]; Fig. 1, item 104), wherein one of the processing units has a control port from which it is to send information to the DMA unit about setting up a DMA channel through which one of data to be consumed and result data by one of the processing units is transferred (see paragraph [0042]; Fig. 9).

Claim 17 relates to a system. The system comprises: a host controller (see paragraph [0019]); external memory (see paragraph [0020]; Fig. 1, item 120); a data driven processor having a memory access unit to interface the external memory, a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit, and a host interface unit to receive instructions from the external host controller that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory, wherein one of the processing units has a control port which it uses to write data location information to the memory access unit (see paragraphs [0017], [0019], and [0026]; Fig. 1,

item 104); and one of a rechargeable battery and a fuel cell coupled to power the external memory, the host controller, and the data driven processor (see paragraph [0031]; Fig. 3, item 330).

Claim 23 relates to a system. The system comprises: external memory (see paragraph [0020]; Fig. 1, item 120); a data driven processor having a memory access unit to interface the external memory, a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit, and a central processing unit to receive and execute instructions that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory, wherein one of the processing units has a control port which it uses to write data channel information to the memory access unit (see paragraphs [0017], [0019], and [0026]; Fig. 1, item 104); and one of a rechargeable battery and a fuel cell coupled to power the external memory and the data driven processor (see paragraph [0031]; Fig. 3, item 330).

Claim 27 relates to a data processor. The data processor comprises: means for translating higher level read and write commands into lower level memory access commands (see paragraphs [0020] and [0021]; Fig. 1, item 132); a plurality of means for consuming data (see paragraphs [0019], [0027], [0031]; Fig. 1, item 104); means for implementing programmable data paths to supply data to and accept data from any one of said plurality of data consumption means (see paragraph [0027]); means for receiving instructions, from other than said plurality of data consumption means, to configure the programmable data path implementation means, the plurality of data consumption means, and the higher level read and write translation means (see paragraphs [0023]-[0026]); and means for implementing a programmable control path through said plurality of data consumption means to transfer higher level read and

write commands from one of said plurality of data consumption means to the higher level read and write translation means(see paragraphs [0023]-[0026]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-9 and 11-29 stand rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,410,723 issued to Schmidt ("Schmidt") in view of U.S. Patent No. 7,729,711 issued to Okamoto ("Okamoto").

All of the claims do not stand or fall together. The basis for the separate patentability of the claims is set forth below.

VII. ARGUMENT

A. Overview of the Cited References

1. Schmidt

Schmidt discloses a wave front array processor that is data driven, and has a number of individual cells which are interconnected with each other and that can be programmed with instructions for processing incoming data and producing result data. See Schmidt, Abstract. Additionally, each cell of the array processor of Schmidt includes handshake ports to perform communications with adjacent cells. See Schmidt, Column 3, Line 50 through Column 4, Line 10. Although the ports in Schmidt are used to transfer data, they are not used to transfer data for the establishment of a data channel. Instead, the handshake ports of Schmidt are merely used to interface between adjacent cells.

2. Okamoto

Okamoto discloses a data driven processor that can read and write from an external main memory. See Okamoto, Column 2, Line 56 through Column 3, Line 4. Okamoto describes how the data driven processor can be interfaced to the external

main memory with the use of an address translation table to maintain cache coherence between the data driven processor and the external main memory. See *Id.*

B. Claims 1-9 and 11-29 Rejected Under 35 U.S.C. § 103(a)

Claims 1-9 and 11-29 stand rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,410,723 issued to Schmidt ("Schmidt") in view of U.S. Patent No. 7,729,711 issued to Okamoto ("Okamoto"). Schmidt and Okamoto, alone or in combination, do not teach or suggest all the claim limitations.

In regard to claim 1, this claim involves a first processing unit which instigates the transfer of data to an external memory unit of a data driven processor through a secondary processing unit. In particular, independent claim 1 recites "the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second processing unit via said data path" (emphasis added). Schmidt and Okamoto, alone or in combination, fail to teach or suggest these aspects.

The Examiner contends that Schmidt discloses each limitation of claim 1 except for a processing unit being connected to external memory. See Final Office Action mailed October 14, 2008, pages 3, 14, and 15. The Examiner argues that Okamoto discloses these aspects at Figures 5, 6, and 7. See *Id.* The Examiner concludes that the combination of Schmidt and Okamoto disclose the recited elements of claim 1. The Appellants respectfully disagree with this contention.

Schmidt discloses a wave front array processor that is data driven, and has a number of individual cells which are interconnected with each other. Each cell can be programmed with instructions for it to process its incoming data and produce result data. While Okamoto does describe how a data driven processor can be interfaced to an external main memory. Okamoto is only focusing on the interface between the **outer periphery** of the processor and external memory, no the core individual processing units or cells. The memory addressing information is assumed to appear, some how, at

the outside interface of the data driven processor. Okamoto does not teach or suggest how any one of its several processing units (or cells) responds to its programmed instructions. Accordingly, Okamoto does not teach or suggest *a first processing unit, in response to recognizing that a first set of instructions received by the first processing unit will require one of reading from and writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and a second processing unit via said data path.*

In view of at least the foregoing, it is readily apparent that Schmidt and Okamoto, alone or in combination, do not teach or render obvious claim 1.

As to claim 5, neither Schmidt or Okamoto suggest a data processor having a number of processing units coupled to each other as recited in the claim, and wherein *one of the processing units has a control port from which it is to send information to a DMA unit of the data processor about setting up a DMA channel through which data to be consumed or result data by one of the processing units is transferred.* In Schmidt, handshake ports of adjacent cells communicate with each other to transfer incoming and result data between those adjacent cells only. There is no suggestion of Appellants' claimed *control port.*

As to Okamoto, there a cache memory unit CM is provided between a memory interface unit VM and a data driven processor PE (see Fig. 5 of Okamoto). A data packet that includes an address of the main memory is provided by the processor, for example, as part of a write or read instruction. Okamoto does not teach or suggest modifying a processing cell or a processing element within the data processor of Schmidt or Okamoto, to provide the cell with *a control port from which it is to send information to a DMA unit about setting up a DMA channel through which data to be consumed or result data by one of the cells is transferred.* Appellants' claim 5 modifies the *processing unit* with the claimed *control port* as recited, making the *processing unit* aware of the location from which data is read to be consumed, or to which result data is to be written. As neither Schmidt nor Okamoto teach or suggest such capability for a constituent cell or processing element of a data driven processor, Schmidt and

Okamoto, alone or in combination, do not render obvious Appellants' independent claim 5.

As to claim 17, this claim recites a system in which a data driven processor has a memory access unit and a number of processing units having the capability recited, as well as being coupled to each other as recited, where *one of the processing units has a control port which it uses to write data location information to the memory access unit.* Neither Schmidt nor Okamoto teach or suggest that an individual processing cell or unit that makes up a data driven processor be provided with such a capability. The processing cells or elements of the Schmidt and Okamoto processors do not write data location information to the necessary access unit; they only accept incoming data (and produce result data) without recognizing or having knowledge of any initial or final memory location or address associated with that data.

Thus, it is readily apparent that Schmidt and Okamoto, alone or in combination, do not teach or suggest all the claim limitations of independent claim 17.

As to claim 23, this claim recites a system in which a data driven processor has a memory access unit and multiple processing units, each coupled to each other as recited, and wherein *one of the processing units has a control port which it uses to write data channel information to the memory access unit.* Neither Schmidt nor Okamoto teach or suggest that an individual processing cell or unit that makes up a data driven processor be provided with such a capability.

Thus, it is readily apparent that Schmidt and Okamoto, alone or in combination, do not teach or suggest all the claim limitations of independent claim 23.

Finally, claim 27 is recited in means plus function format and includes a *means for implementing a programmable control path through multiple data consumption means, to transfer higher level read and write commands from one of the data consumption means to a higher level read and write translation means.* Once again, the Office Action does not adequately present the basis for its rejection of this claim, by, for example, mapping the

various limitations of Applicants' claim 27 to corresponding elements in the prior art. The Final Office Action at page 16 merely recites that Schmidt/Okamoto disclose a data processor as recited, referring only to passages in the text that are not helpful in determining how the Examiner is interpreting the claim limitations.

For instance, the Appellants are left wondering what elements in the prior art does the limitation *means for implementing a programmable control path through the plurality of data consumption means to transfer higher level read and write commands from one of the data consumption means to the higher level read and write translation means* read on. The Final Office Action refers to memory instructions of Schmidt/Okamoto that require the use of switching data streams which are considered to be the lower level memory access command. But no conclusion can be drawn from that statement.

The "memory instructions" described in Schmidt are different than those that are of concern in Okamoto. The instructions in Okamoto are designed to interface the data driven processor to external memory. The instructions in Schmidt are designed to program individual cells. There needs to be further explanation of how a person having ordinary skill in the art would understand such instructions as being used in the manner recited in Applicants' claim 27. No such explanation has been given in the Office Action. Accordingly, it is respectfully submitted that the case made for rejecting the claims in the Final Office Action is improper in that it does not fairly apprise Appellants of the basis for the rejection.

Thus, it is readily apparent that the Examiner has failed to establish how Schmidt and Okamoto, alone or in combination, teach or suggest all the claim limitations of independent claim 23.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

For the reasons set forth above, the Appellants respectfully request the Board overturn the rejections of claims 1-9 and 11-29.

Respectfully submitted,

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Dated: 20 April, 2009

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Jessica Huester — Date 4/20/09

VIII. CLAIMS APPENDIX

The claims involved in this Appeal are as follows:

1. (Original) A data driven processing method, comprising:

providing a first set of instructions and incoming data to a first processing unit, of a data driven processor, to operate upon said incoming data;

configuring a data path for transferring data between a second processing unit of the data driven processor and external memory; and

the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second processing unit via said data path.

2. (Original) The method of claim 1 wherein the first processing unit recognizes an image processing motion vector in said first set of instructions, and said additional data is to be written to the external memory and includes a macro block generated by the second processing unit based on the motion vector.

3. (Original) The method of claim 1 wherein the data path is configured by an external host controller.

4. (Original) The method of claim 1 further comprising:

the first processing unit providing an indication to the memory access unit of whether the transfer is one of a read and a write.

5. (Previously Presented) A data processor comprising:

a first direct memory access (DMA) unit; and

a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one

of the processing units to another and from any one of the processing units to the DMA unit, the plurality of processing units are essentially identical units each having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port wherein the input port is programmable to route incoming data to any one of the output ports,

wherein one of the processing units has a control port from which it is to send information to the DMA unit about setting up a DMA channel through which one of data to be consumed and result data by one of the processing units is transferred.

6. (Original) The processor of claim 5 further comprising:

memory interface circuitry, wherein the DMA unit is to access external memory via the memory interface circuitry.

7. (Previously Presented) The processor of claim 6 further comprising a host interface through which a host processor is to configure data flow between the data ports, wherein the memory interface circuitry is on-chip with the DMA unit, the plurality of processing units, and the host interface.

8. (Original) The processor of claim 6 wherein the memory interface circuitry is designed to interface with external memory that is dynamic random access memory.

9. (Previously Presented) The processor of claim 5 wherein each of the processing units has an input programming element (PE) to read incoming data from any one of its input ports, an output PE to write result data to any one of its output ports, and a core PE to execute instructions independently of a data path that is operating through a pair of the input and output ports of that processing unit.

10. Canceled.

11. (Previously Presented) The processor of claim 6 wherein each of the plurality of processing units has a plurality of control ports on each side including an

input control port and an output control port, and wherein the input control port of a processing unit is programmable to route incoming command information to any one of the output control ports of said processing unit.

12. (Original) The processor of claim 9 further comprising an interface to an external device, and wherein the output ports of one of said processing units are coupled to the input ports of an adjacent one of said processing units except that some of the output ports of an outlying one of said processing units are coupled to the external device interface.

13. (Previously Presented) The processor of claim 5 further comprising:

a second DMA unit, wherein there are at least four of said plurality of processing units, the data ports on a north side of first and second ones of said four processing units are coupled to the first DMA unit, the data ports on a south side of third and fourth ones of said four processing units are coupled to the second DMA unit, and the data ports of a south side of the first and second processing units are coupled to the data ports of a north side of the third and fourth processing units.

14. (Original) The processor of claim 13 further comprising an interface to an external device, wherein some of the data ports of east and west sides of the processing units are coupled to the external device interface.

15. (Original) The processor of claim 5 further comprising a central processing unit to read and execute instructions that configure the data ports and the DMA unit to create a data channel from one of the processing units to external memory.

16. (Original) The processor of claim 5 further comprising a host interface unit to receive instructions, from an external host controller, that configure the data ports and the DMA unit to create a data path from one of the processing units to external memory.

17. (Original) A system comprising:

a host controller;

external memory;

a data driven processor having a memory access unit to interface the external memory, a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit, and a host interface unit to receive instructions from the external host controller that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory, wherein one of the processing units has a control port which it uses to write data location information to the memory access unit; and

one of a rechargeable battery and a fuel cell coupled to power the external memory, the host controller, and the data driven processor.

18. (Original) The system of claim 17 wherein the host controller includes an embedded processor and its associated main memory.

19. (Original) The system of claim 17 wherein the coupling of each pair of data ports from adjacent processing units is a point-to-point, unidirectional connection.

20. (Original) The system of claim 19 wherein each of the processing units has a core programming element (PE) that can be programmed to execute instructions that operate on incoming data received via an input data port of that processing unit, an input PE that can read data from any one of a plurality of input data ports of that processing unit, and an output PE that can write data to any one of a plurality of output data ports of that processing unit.

21. (Original) The system of claim 20 wherein the core PE of each processing unit can execute its instructions independently of a data path that is operating through a pair of said input and output data ports of that processing unit.

22. (Original) The system of claim 17 wherein the data location information that is sent through the control port includes information about the size and display location of a block of image data.

23. (Original) A system comprising:

external memory;

a data driven processor having a memory access unit to interface the external memory, a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit, and a central processing unit to receive and execute instructions that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory, wherein one of the processing units has a control port which it uses to write data channel information to the memory access unit; and

one of a rechargeable battery and a fuel cell coupled to power the external memory and the data driven processor.

24. (Previously Presented) The system of claim 23 wherein each of the processing units has a plurality of control ports that are connected to each other in a mesh arrangement so that the data channel information, including one of a read and write command, address, and memory access unit channel identifier, can originate from any one of the processing units and be routed to the memory access unit via a logical control channel programmed in the mesh arrangement.

25. (Original) The system of claim 23 wherein the coupling of each pair of data ports from adjacent processing units is a point-to-point, unidirectional connection.

26. (Original) The system of claim 23 wherein each of the processing units has a plurality of control ports that are coupled to each other and are programmable to

allow data channel information to be sent from any one of the processing units to the memory access unit.

27. (Previously Presented) A data processor comprising:

means for translating higher level read and write commands into lower level memory access commands;

a plurality of means for consuming data;

means for implementing programmable data paths to supply data to and accept data from any one of said plurality of data consumption means;

means for receiving instructions, from other than said plurality of data consumption means, to configure the programmable data path implementation means, the plurality of data consumption means, and the higher level read and write translation means; and

means for implementing a programmable control path through said plurality of data consumption means to transfer higher level read and write commands from one of said plurality of data consumption means to the higher level read and write translation means.

28. (Original) The processor of claim 27 further comprising means for ensuring that said lower level memory accesses meet signal level and timing requirements of external memory.

29. (Original) The processor of claim 27 further comprising means for expanding the data processor.

IX. EVIDENCE APPENDIX

No evidence is submitted with this appeal.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings exist.

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